REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

Applicant submitted an Information Disclosure Statement on March 31, 2004. Consideration of that Information Disclosure Statement by returning the initialed PTO-1449 forms is respectfully requested.

The Examiner requests copies of two IBM Technical Disclosure Bulletins and relevant excerpts from three text books. An Information Disclosure Statement providing this information requested by the Examiner will be filed shortly.

The drawings stand objected to as failing to comply with 37 CFR §1.84(p)(4), noting an inconsistency with reference numerals 64 and 68. Attached hereto is a replacement sheet for Figure 9 in which the reference numeral for the Java bytecode translation block has been relabeled with reference numeral 64 consistent with the Java bytecode translator 64 shown in Figure 3.

The description of Figure 9 has also been amended to make this same correction. Acceptance of the replacement sheet and withdrawal of the objection to the drawings are respectfully requested.

The Examiner objects to the Abstract citing inconsistencies in the reference characters. A new abstract has been submitted with reference characters removed from the Abstract. Withdrawal of the objection to the Abstract is requested.

The Examiner objects to the disclosure noting a few misspellings. They have been corrected by amendment. Withdrawal of the objection to the specification is respectfully requested.

Claims 1, 11-13, and 14-16 stand rejected under 35 §103 as being unpatentable over U.S. Patent 6,513,057 to McCrory and U.S. Patent 6,564,179 to Belhaj. This rejection is respectfully traversed.

McCrory discloses a heterogeneous, symmetric, multi-processor (HSMP) computer system having two or more processors that share memory and I O devices, the processors having different native instruction sets. An HSMP operating system controls scheduling operations on the HSMP system by maintaining separate "ready" queues for each different family of processors. The system enables different sets of instructions within a single thread to execute on processors belonging to different families. When a thread is created, the operating system determines an initial processor family to associate with the thread based on the binary code that the thread will begin executing. During execution of the thread, the operating system may reschedule a given set of instructions to a processor of a different family for execution. The thread is then returned to a processor in the previous family.

The Examiner admits that "McCrory does not teach a software-based instruction execution unit for which program instructions are to be sent if not supported by hardware based execution unit." See elements (ii) and (iv) of claim 1. But in addition, McCrory fails to disclose a hardware based instruction unit that:

> includes scheduling support logic operable to generate a scheduling signal for triggering a scheduling operation to be performed between program instructions irrespective of whether a proceeding program instruction was executed by said hardware based execution unit or said software based execution unit.

In contrast, McCrory describes that when a thread is created, the "HSMP OS determines the initial processor family to associate with that thread, based on the binary code stream that the thread will begin executing." Column 8, lines 12-15. That initial processor family is determined from plural distinct hardware processor families as shown in Figure 3. Consequently, not all program instructions are sent to a given hardware based instruction unit in McCrory's system.

The differences between claim 1 and McCrory result in significant benefits. The apparatus of claim 1 can better support scheduling operations with less likelihood that data integrity will be compromised due to a context switch during a scheduling operation. Furthermore, there is no need in the apparatus of claim 1 to exchange program counter values between two sets of program instructions. Thus, the problem addressed by the present invention is to enable more reliable support for scheduling operations in a system where program instructions may be executed on one of plural instruction execution units.

Based on McCrory's teachings and faced with the problem of providing more reliable support for scheduling operations, (in a system where program instructions may be executed on one of a plurality of instruction execution units), a person of ordinary skill in the art would realize that for a given program execution thread, scheduling operations could be supported for that thread using scheduling support logic on the particular

processor corresponding to which that thread was initially allocated for execution. But because McCrory initially allocates different threads to **different** processors, the problem remains of reliable overall control of scheduling operations without the need to exchange program counter values between the different families of processors P1, P2,...Pn (see McCrory Figure 1 and the Abstract).

The Examiner attempts to rely on Belhaj to remedy at least the admitted deficiency (although McCrory suffers from more than just the admitted deficiency as explained above). Belhaj discloses a single processor system that combines the functions of two types of processors such as a digital signal processor (DSP) and a microcontroller. The system incorporates a software-based run-time emulation module of a particular processor (e.g., a microcontroller) within the hardware core of a different processor (the host processor, e.g., a DSP). The emulation module allows both DSP code and microcontroller control code to execute independently on the host processor by time division multiplexing of processing resources. Belhaj addresses problems associated with combining the functions of two types of processors.

Belhaj does **not** teach that program instructions unsupported by a hardware-based instruction execution unit are first sent to the hardware-based execution unit and then forwarded to a software-based execution unit as specified in elements (ii) and (iv) of claim 1. Nor does Belhaj disclose the hardware-based execution unit triggering scheduling operations between program instructions regardless of whether that program instruction was an emulated program instruction or a host processor program instruction,

to element (v) of claim 1. Thus, neither McCrory nor Belhaj discloses elements (ii), (iv), and (v) of claim 1.

To combine the functions of two types of processors, Belhaj teaches incorporating a software-based, run-time emulation module of a particular processor (e.g., a microcontroller) within the hardware core of a different processor (e.g., a DSP). Belhaj also teaches that program code associated with the DSP is stored in a first portion of program memory, whereas program code associated with the emulated processor is stored in a second portion of program memory. Column 2, lines 42-49. A host line of program code is retrieved and executed for the DSP, and a **distinct** emulated line of program code is retrieved and executed for the run-time emulation module. At column 4, lines 28-31, ***distinct program counters*** are used for the emulation program code and for the program code of the host processor.

Accordingly, Belhaj *teaches away* from claim 1. In particular, Belhaj's system *requires* exchanging counter values between the host processor executed program instructions and the emulation module executed program instructions. That exchange leads to the same disadvantage associated with the prior art described on page 2, lines 31-34 of the present application. Thus, even the teachings of McCrory and Belhaj were combined, (for purposes of argument only), those combined teachings would not suggest all the elements of claim 1.

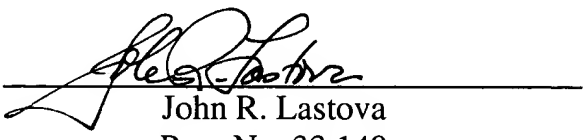
Lacking multiple features of independent claim 1 and analogous figures in independent method claim 16, the rejection of the claims based upon the combination of

McCrory and Belhaj should be withdrawn. Although claims 2-10 stand rejected under 35 U.S.C. §103 as being unpatentable over McCrory and Belhaj in view of "Applicant's admitted prior art," any alleged admitted prior art fails to overcome the deficiencies identified above with respect to McCrory and Belhaj in the independent claims.

The application is in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 
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